Simulation of Single-Phase Cascade Multilevel PWM Inverters

Adrian Şchiop*, Felicia Şchiop**
* Department of Electronics,
University of Oradea, Faculty of Electrical Engineering and Information Technology,
Universităţii str., no. 1, 410108 Oradea, Romania, E-Mail: aschiop@uoradea.ro

**Lucian Blaga High School, Oradea
Aleea Posada str., no.1, 410364, Oradea

Abstract ***– This paper presents simulation of a single – phase cascade multilevel PWM inverter topology. Solution is based on series connection of 3 level diode clamped inverters modules and flying capacitor inverter modules, which gives possibility for flexible operation of inverter at various high voltage.***

Keywords: ***cascade multilevel PWM inverter, flying capacitor inverter, diode clamped inverter.***

I. INTRODUCTION

Multilevel power conversion has been receiving increasing attention in the past few years for high-power applications [1]. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literature. These inverters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating.
In the family of multilevel inverters, topologies based on series-connected H-bridges are particularly attractive because of their modularity and simplicity of control. It gives high flexibility to extend inverter to more legs or high number of level as well as it minimize total harmonic distortion THD, that can provide reduction of output filters.
This paper describes simulation study of single-phase cascade multilevel PWM inverters based on 3 level diode clamped modules and 3 level flying capacitor modules. A comparison between two topologies is made regarding THD. The influence on the THD of the disposition of the carrier signals is also investigated.
The paper is organized as follows. Section II describes the 3, and 9 level inverters and the simulation models for diode clamped inverter and flying capacitor inverter with examples of modulation for each inverter. Section III presents simulation study in Simulink environment as well as THD voltage for all cascade inverters.

II. DESCRIPTION OF MULTILEVEL CASCADE PWM INVERTER

A. 3 level diode clamped inverter

Circuit diagram for a 3 level diode clamped inverter is presented in Fig. 1. The model of the *n* level diode clamped inverter based on "n" position switches was described in [2]. For 3 level diode clamped inverter this model shows like in Fig. 2.

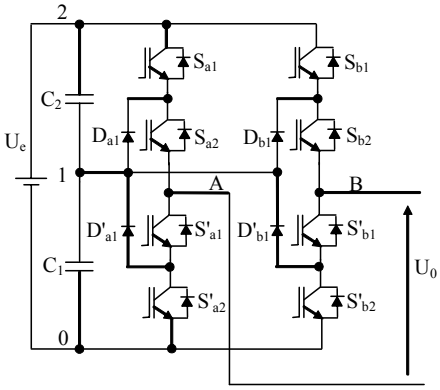

Fig. 1 Circuit diagram for the 3 level diode clamped inverter.

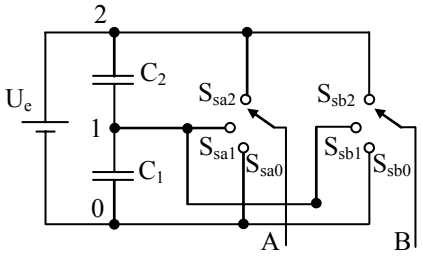

Fig. 2 Equivalent model of the 3 level diode-clamped inverter based on "n" position switches.

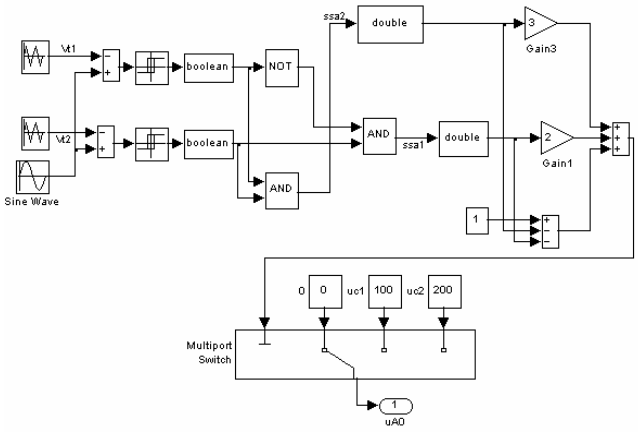

Fig. 3 Simulink model for phase voltage for 3-level inverters.

In Fig. 3 one can see the presence of a multiport switch set for a 3-level inverter. The circuit offers the output voltage for a single leg. The phase voltage u_{A0} is given by (1):

$$u_{A0}=s_{sa1}u_{c1}+s_{sa2}(u_{c1}+u_{c2}) \quad (1)$$

where s_{sa1} and s_{sa2} are the commutation functions defined in [2].

B. 3 level flying capacitor inverter

For the 3 level flying capacitor inverter the two switches S_{xi} and S'_{xi} from Fig. 4 are driven complementary. An inverter leg may be represented as in Fig. 5.

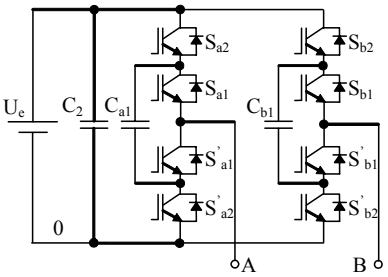

Fig. 4 Circuit diagram for the 3 level flying capacitor.

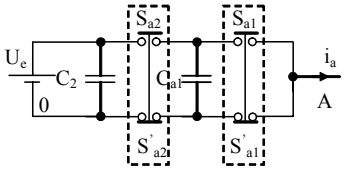

Fig. 5 Modeling of inverter leg flying capacitor inverter.

The phase voltage u_{a0} depend on connection functions y_{a1} and y_{a2} is derived in [3]:

$$u_{A0}=y_{a2}u_{Ca2}+u_{Ca1}(y_{a2}+y_{a1})[(1-y_{a2})+(1-y_{a1})](-1)^{(1-ya1)} \quad (2)$$

Simulink model of flying capacitor multilevel inverter, presented in Fig. 6, employs the following blocks of the Simulink library: *Source, Sum, Relay, Constant, Gain, Product* and *Math Function*. The *Triangle block* is a mask subsystem that allows set up of the amplitude, frequency, phase and offset of carrier signals. The *Math* blocks realizes the $(-1)^{(1-ya1)}$ operations. The *Gain* blocks multiplies the values of connection functions with values of voltages on flying capacitors.

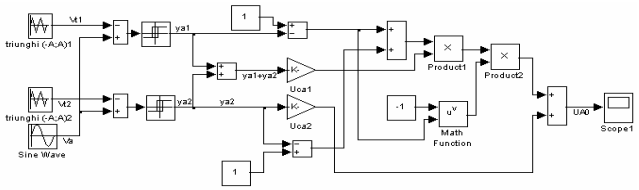

Fig. 6 Simulink model of the four level flying capacitor inverter.

C. 9 level inverter

Fig. 7 presents 9 level cascade diode-clamped inverter assembled from two modules of 3 level diode-clamped inverters and Fig. 8 presents 9 level cascade flying capacitor inverter assembled from two modules of 3 level flying capacitor inverters.

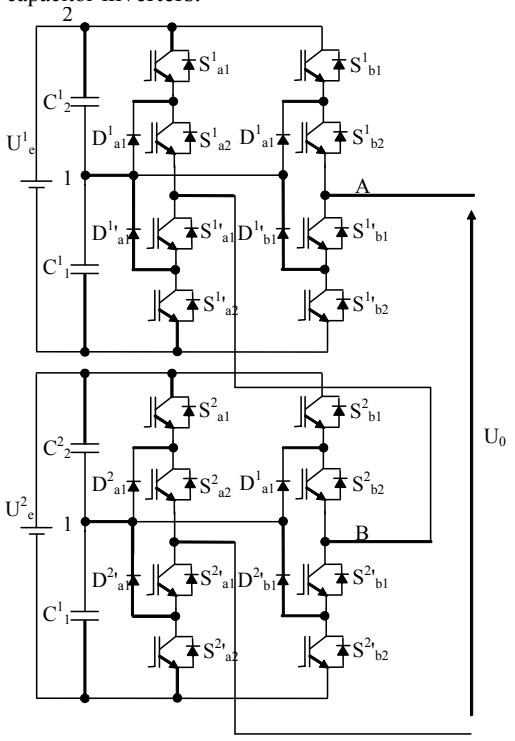

Fig. 7 Scheme of 9 level cascade diode clamped inverter.

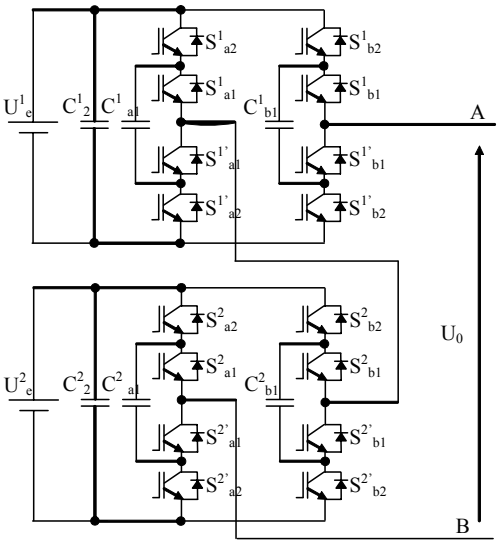

Fig. 8 Scheme of 9 level cascade flying capacitor inverter.

The output voltage of cascade multilevel inverters presented in Fig. 7 and Fig. 8 is:

$$u_{AB}=U_e^1 y_1+U_e^2 y_2\ ;\ y_1, y_2=\{1, 1/2, 0, -1/2, -1\} \quad (3)$$

where y_1, and y_2 are the switching functions defined in [5] In [3], [4] it has been shown that the THD value of output voltage of diode clamped multilevel inverter is smallest when the carrier signals are in phase covering a continuous domain. For flying capacitor multilevel inverter the small values of THD is obtained when carrier signals are common for two leg and they are in phase, mode A, or when carrier signals are phase shifted mode B [2]. For

cascade multilevel inverters will be study if this modulation techniques allow obtaining the lowest value of THD.
In Fig. 9 the nine levels of the output voltage of the inverter can be obtaining. The output levels of the upper cell are U_e, $U_e/2$, 0, $-U_e/2$ and $-U_e$, while for the lower cell the output levels are: U_e, 0, $-U_e$. By combination of the two sets of output values, the output voltage of the cascade inverter would have nine values: $2U_e$, $3U_e/2$, U_e, $U_e/2$, 0, $-U_e/2$, $-U_e$, $-3U_e/2$ and $-2U_e$.

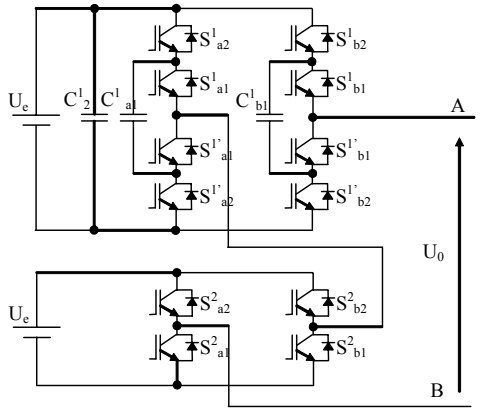

Fig. 9 Scheme of 9 level hybrid multilevel inverter.

III. SIMULATION RESULTS

The simulation is realized using Simulink models presented in Fig 3 and Fig. 6.
The THD are calculated for the first 200 harmonics. The amplitude modulation index is 0.9, the switching frequency is f_p=1250 Hz and DC link voltage U_e=200V. The frequency of the modulating signals is 50 Hz and the frequency modulation index is 25.
For the cascade flying capacitor with 9 level, mode A, the carrier signals for the two blocks are phase shifted by $T_p/2$, where T_p is the switching time.

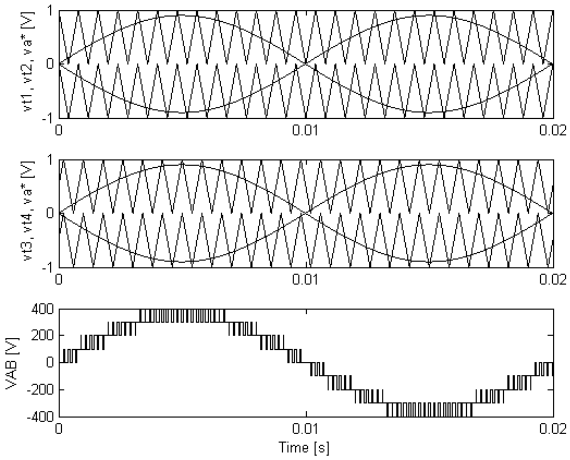

Fig. 10 A mode for 9 level cascade flying capacitor. From the top: reference voltage with carrier voltages, output voltage of inverter,

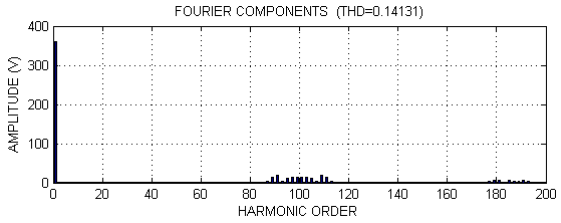

Fig. 10 Harmonic amplitude for A mode for 9 level cascade flying capacitor.

One can see that for A mode, the harmonics of voltage line appear as side bands of frequency f_{hA}:

$$f_{hA}=4f_p; \quad (4)$$

For the cascade flying capacitor with 9 level, mode B, presented in Fig. 10, the carrier signals v_{t1} and v_{t2} are for the upper block while v_{t3} and v_{t4} are for the down block. v_{t1} and v_{t3} are phase shifted by $T_p/2$.
One can see from Fig. 10 that (4) remain valid but THD is almost double confronted by previous case.
For A mode is analyzed the situation when the two blocks have not the same voltage supply. In Fig. 11 is presented the situation when the voltage supply for one block is double confronted by the other block. For this case the voltage V_{AB} has 13 levels but the THD is grater than 9 level cascade flying capacitor is used. For 13 levels inverter the harmonics are grouped around the double switching frequency.

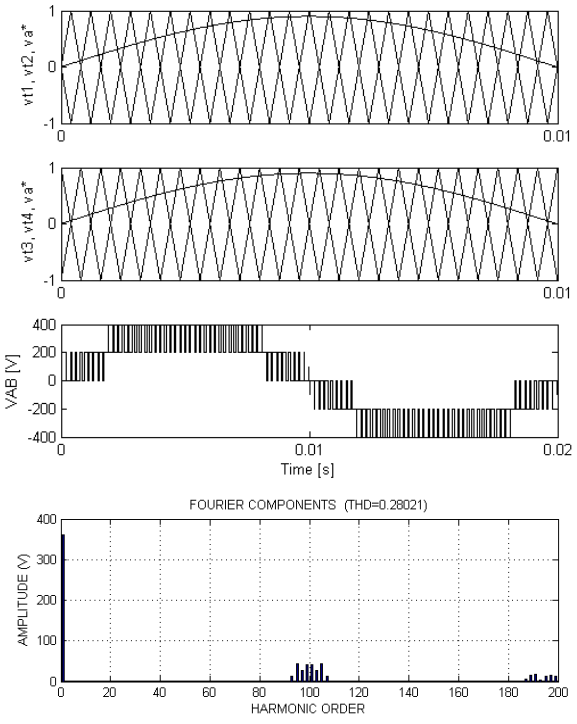

Fig. 11 B mode for 9 level cascade flying capacitor.

The lowest values of THD, 0.141, are obtained for A mode. For B mode it was obtained 0.28.

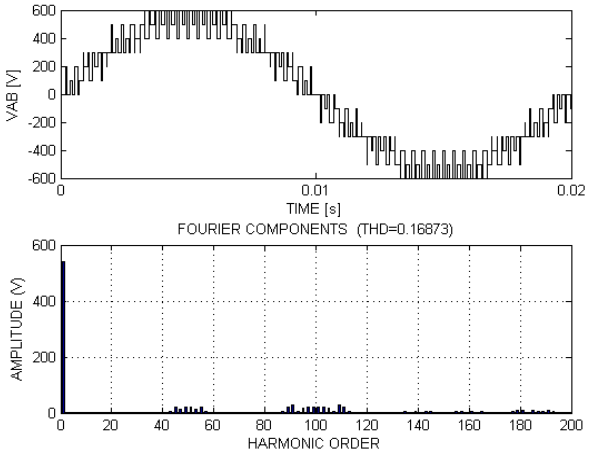

Fig. 12 A mode for 13 level cascade flying capacitor inverter

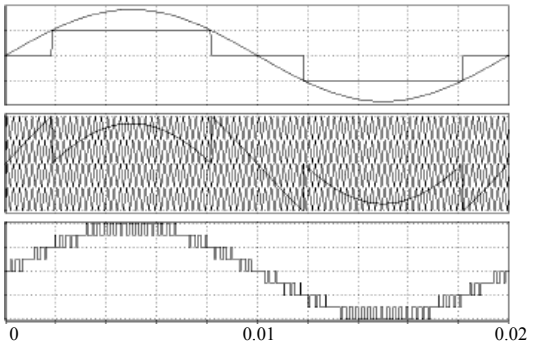

Fig. 13. Modulation in 9-level inverter. From the top: reference voltage with switching function for bottom converter, reference voltage with carrier signals for upper inverter, output voltage of inverter

IV. CONCLUSIONS

This paper presents single-phase cascade multilevel PWM inverters based on 3 level diode clamped modules and 3 level flying capacitor modules. A comparison between two topologies is made regarding THD. The influence on the THD of the disposition of the carrier signals is also investigated..

REFERENCES

[1] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," IEEE Tran. on Ind. Electro., vol. 54, no. 6, pp. 2930–2945, December 2007.

[2] A. Şchiop, ″Simulink Model of Flying Capacitor Multilevel Inverter″ Proceedings of OPTIM 2008 vol.2. pp. 203 – 208.

[3] A. Şchiop, D. Trip "Simulink Models of Single Phase Multilevel Inverters" Conference Proceedings of National Symposium of Theoretical Electrical Engineering SNET'07, Bucuresti, 2007, pp. 254–260.

[4] A. Şchiop, D. Trip, V. Fedak Contribution to Modelling of Diode-Clamped Multilevel Inverters Conference proceedings from the 16th International Conference on Electrical Drives and Power Electronics Hight Tatras Slovakia, CD

[5] A. Şchiop, Contributions to the Study of the Converters Used to the Asynchronous Motor Drives, Ph.D. Thesis, "Politehnica" University of Timisoara, January 2007